



Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT620T/AT/CT
IDT54/74FCT623T/AT/CT

FEATURES:

- Std., A and C speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA I_{OH} , 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION

The IDT54/74FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

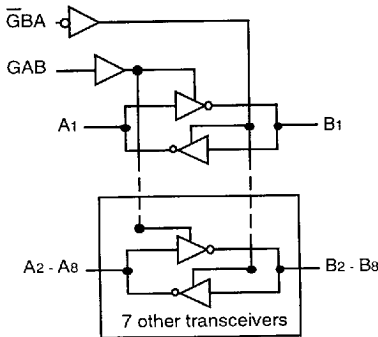
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the IDTFCT620T/AT/CT and IDTFCT623T/AT/CT is the Power Down Disable capability. When the $\overline{\text{GAB}}$ and $\overline{\text{GBA}}$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when $V_{CC} = 0\text{V}$. This is a desirable feature in back-plane applications where it may be necessary to perform "live" insertion and removal of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

The IDTFCT620T/AT/CT is the inverting option of the IDTFCT623T/AT/CT.

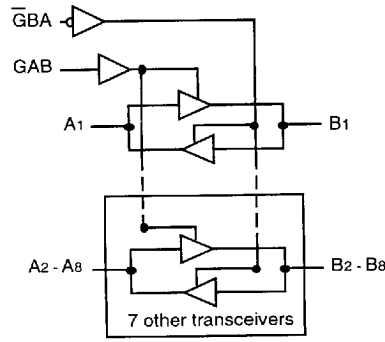
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FUNCTIONAL BLOCK DIAGRAMS



FCT620T/AT/CT

2563 drw 01



FCT623T/AT/CT

2563 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

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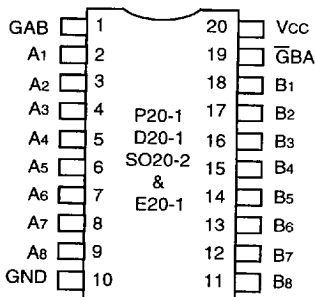
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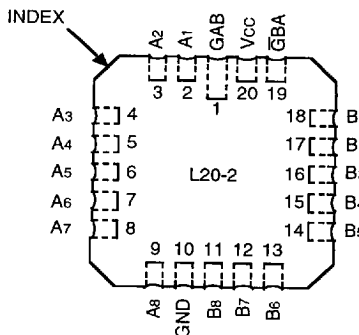
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PIN CONFIGURATIONS



**DIP/SOIC/CERPACK
TOP VIEW**

2563 drw 03



**LCC
TOP VIEW**

2563 drw 04

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{G}BA, GAB$	Enable Inputs
A1 - A8	A Bus Inputs or 3-State Outputs
B1 - B8	B Bus Inputs or 3-State Outputs

2563 tbl 01

FUNCTION TABLE⁽¹⁾

Enable Inputs		Outputs	
$\overline{G}BA$	GAB	FCT620	FCT623
L	L	\overline{B} data to A bus	B data to A bus
H	H	\overline{A} data to B bus	A data to B bus
H	L	Z	Z
L	H	\overline{B} data to A bus \overline{A} data to B bus	B data to A bus A data to B bus

NOTES:

1. H = HIGH Voltage Level
2. L = LOW Voltage Level
3. Z = High-Impedance (OFF) state

2563 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	-0.5 to $V_{CC}+0.5$	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

2563 lmk 03

CAPACITANCE ($T_A = +25^\circ\text{C}, f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

2563 lmk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁵⁾	$V_{CC} = \text{Max.}$, $V_I = 2.7\text{V}$		—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁵⁾	$V_{CC} = \text{Max.}$, $V_I = 0.5\text{V}$		—	—	± 1	μA
I_I	Input HIGH Current ⁽⁵⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = \text{GND}$		-60	-120	-225	mA
V_{OH}	Output HIGH Voltage (A and B Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 32\text{mA MIL.}$ ⁽⁴⁾ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
V_{OL}	Output LOW Voltage (B Bus)	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 48\text{mA MIL.}$ ⁽⁴⁾ $I_{OL} = 64\text{mA COM'L.}$	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁶⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$		—	—	± 1	μA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	μA

2563 IBI 05

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
- This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{G}BA = GAB = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{G}BA = GAB = GND$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	1.8	4.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{G}BA = GAB = GND$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3.0	6.0 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	5.0	14.0 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

2563 tbl 07

$I_C = I_{CC} + \Delta I_{CC} DHNT + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } DH$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT620T/AT/CT

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT620T				54/74FCT620AT				54/74FCT620CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPZH tPZL	Output Enable Time G \bar{B} A to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time G \bar{B} A to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

2563 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT623T/AT/CT

Symbol	Parameter	Condition ⁽¹⁾	54/74FCT623T				54/74FCT623AT				54/74FCT623CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPZH tPZL	Output Enable Time G \bar{B} A to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time G \bar{B} A to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

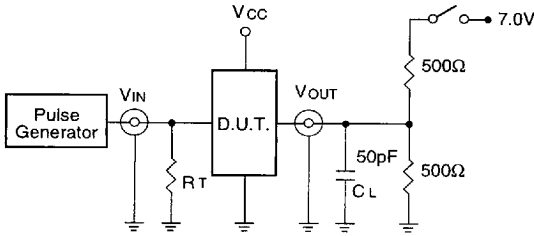
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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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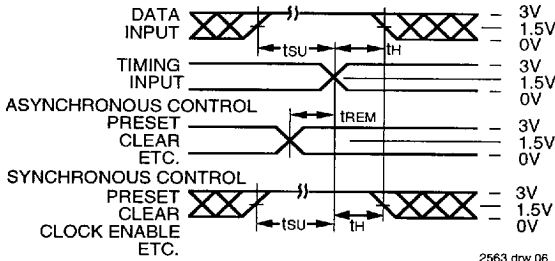
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:
 CL= Load capacitance: includes jig and probe capacitance.
 RT= Termination resistance: should be equal to Zout of the Pulse Generator.

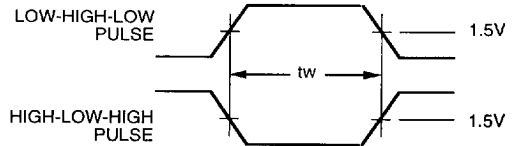
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SET-UP, HOLD AND RELEASE TIMES



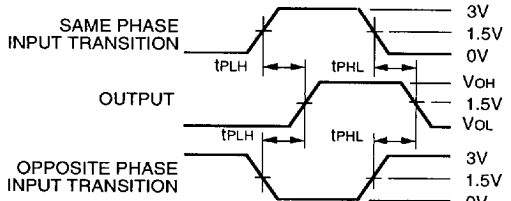
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PULSE WIDTH



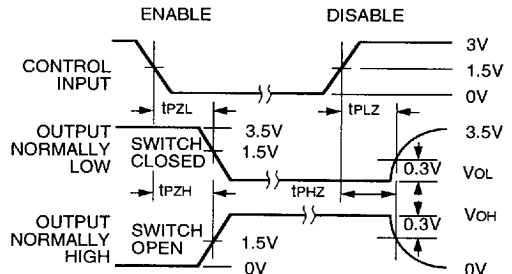
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PROPAGATION DELAY



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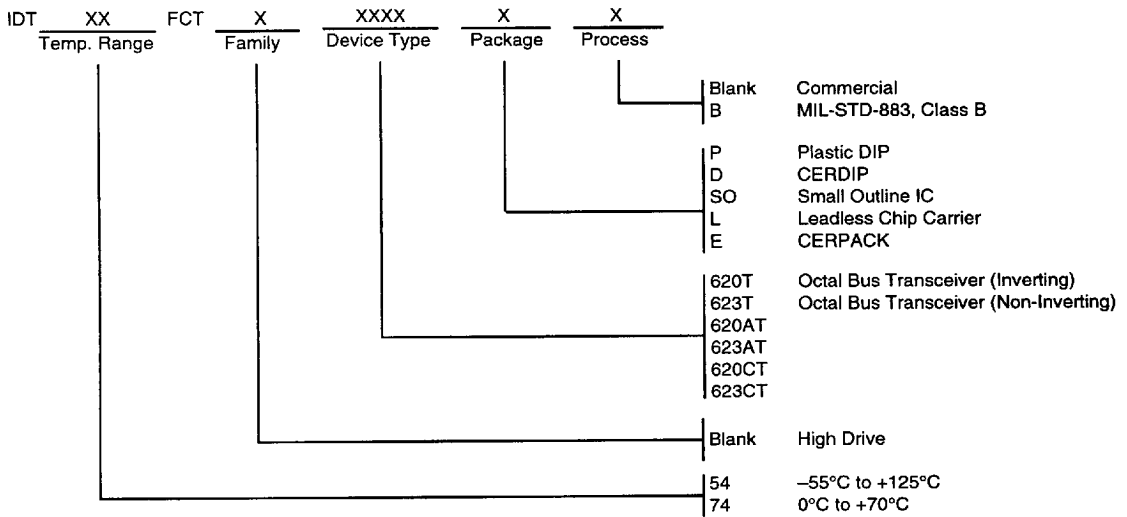
ENABLE AND DISABLE TIMES



2563 drw 09

- NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
 2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; th ≤ 2.5ns

ORDERING INFORMATION



2563 drw 10